

# TSOP I

## Thin Small Outline Package Type I

EEMS offers TSOP I packages to the designers who require a package that is small and thin with end leads.

With a 1.0mm thick body, this package has the short lead lengths for die designs where speed is important: it is available in different body sizes and pin count.

The packages are automatically fully inspected to insure flatness and coplanarity.



## Features & Benefits

- Small board area needed
- Small size
- Cost competitive
- High reliability
- Compliant to Rohs directive 2002/95/CE



## Copper Substrate MATRIX Leadframe

## Applications

Memory, memory and memory are the primary users of this package.

### Device

- SDRAM
- NAND FLASH
- E<sup>2</sup> PROM
- ASIC's

### End Equipment

- Telecom Systems
- Memory Cards
- USB Stickers
- Wireless Base System
- Data Media
- PC Peripherals

## Standard Materials

|                     |                        |
|---------------------|------------------------|
| Substrate           | AL42/Copper Leadframe  |
| Die Attach          | Low stress mtl         |
| Gold wire           | 25-30 um               |
| Mold Compound       | Epoxy                  |
| Lead Solder Plating | 85/15 Sn/Pb or 100% Sn |
| Packing             | Jedec Tray/Tape & Reel |
| Packing option      | Dry Pack               |

## Process Highlights

|                   |                 |
|-------------------|-----------------|
| Processable wafer | 200 – 300 mm    |
| Die Thickness     | 0.280 mm max    |
| Bond Pad Pitch    | 60 um min       |
| Marking           | Laser           |
| Lead inspection   | Auto inspection |

# TSOP I

## Specifications

### Electrical (simulated w/bondwire)

(12 x 18.4 x 1.0 mm body with 48 leads)

Capacitance (pF) : 0.5 - 0.9 at 1 GHz

Inductance (nH) : 3.2 - 4.3 at 1 GHz

Resistance (mΩ) : 200 - 260 at 100 Mhz

### Thermal Resistance (simulated)

(12 x 18.4 x 1.0 mm with 48 leads; 1 Watt, 0 m/s airflow as per JEDEC JESD51.2):

$\Theta_{ja} = 39 \text{ }^{\circ}\text{C/watt}$  Typical

## Reliability

Moisture Sensitivity : JEDEC MSL 3 @ up to 260 °C,

High Temp Storage : 150 °C, 1000 hours

Temp Cycle : -65/+150 °C, 1000 cycles

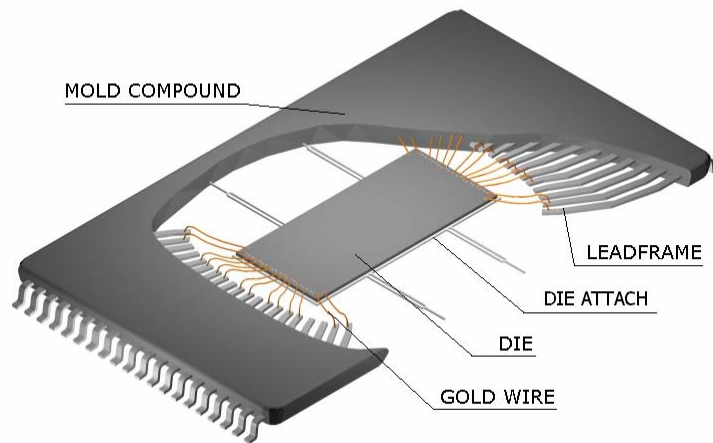
Temp Humidity Test : 130 °C/85% RH, 240 hours HAST

PCT : 121 °C/2 atm., 240 hours

## Available Services

- 300 mm wafer full processing
- Wafer backgrinding
- Wafer map / sort
- Product Engineering
- -30 + 125 °C full test
- Dynamic Burn In
- Compliant to Rohs directive 2002/95/CE

## Cross – Section



TSOP I Nominal Package Dimensions (mm)

| Body Area   | Lead Count | Lead Pitch | Lead edge to edge | Body Thickness | Stand-off | Overall Height | JEDEC  |
|-------------|------------|------------|-------------------|----------------|-----------|----------------|--------|
| 10.0 x 12.4 | 40         | 0.50       | 14.0              | 1.00           | 0.10      | 1.2 max        | MO-142 |
| 8.0 x 18.4  | 32         | 0.50       | 20.0              | 1.00           | 0.10      | 1.2 max        | MO-122 |
| 10.0 x 18.4 | 40         | 0.50       | 20.0              | 1.00           | 0.10      | 1.2 max        | MO-122 |
| 12.0 x 18.4 | 48         | 0.50       | 20.0              | 1.00           | 0.10      | 1.2 max        | MO-142 |